CLAIMS

1. (Previously Presented) A device comprising:

an active region;

a gated device having a gate and a junction region adjacent to the gate within the active region;

a dielectric layer on the gated device having a first thickness over the gate and a second thickness greater than the first thickness over the junction region adjacent to the gate;

a contact in the active region extending a first depth through the first thickness to the gate of the gated device, and extending a different second depth through a portion of the second thickness short of the junction region.

2. (Original) The device of claim 1, wherein the gated device comprises at least one SRAM cell.

3. (Previously Presented) The device of claim 1, wherein the contact is a first contact and the active region further comprises:

a second contact through the dielectric layer to the junction region of the gated device.

4. (Original) The device of claim 3, wherein the dielectric layer comprises a material selected from the group consisting SiO_2, PSG, Si_3N_4, and SiC.

5. (Original) The device of claim 3, wherein the dielectric layer on the gated device further comprises a conformal etch stop layer on the junction region and the gate of the gated device.

6. (Original) The device of claim 5, wherein the conformal etch stop layer comprises a material selected from the group consisting SiO_2, PSG, Si_3N_4, and SiC.

7. (Previously Presented) The device of claim 5, wherein the first contact extends through the dielectric layer and

through the conformal etch stop layer to the gate.

8. (Previously Presented) The device of claim 5, wherein the dielectric layer on the gated device further comprises:

a planarized first dielectric layer in the active region of the gated device exposing the conformal etch stop layer on a portion of the gate;

a different second dielectric layer on the gated device in the active region; and

wherein the first contact extends through the different second dielectric layer, the planarized first dielectric layer, and the conformal etch stop layer to the gate.

9. (Previously Presented) The device of claim 5, wherein the dielectric layer on the gated device further comprises:

a planarized first dielectric layer in the active region of the gated device for exposing the conformal etch stop layer on a portion of the gate;

a second etch stop layer on the first dielectric layer and the conformal etch stop layer;

a second dielectric layer on the second etch stop layer; and

wherein the first contact extends through the second dielectric layer, the second etch stop layer, the planarized first dielectric layer, and the conformal etch stop layer to the gate.

10. (Previously Presented) The device of claim 3, wherein the dielectric layer on the gated device further comprises:

a first partially planarized conformal dielectric layer on the gated device in the active region having a first height on a portion of the junction region which is less than the height of said gate, and having a different second height on a portion of the gate which is substantially less than the first height;

a different second dielectric layer on the gated device in the active region; and

wherein the first contact extends through the different second dielectric and the first partially planarized conformal dielectric layer to the gate.